CLAIMS

We Claim:

1. A method for forming an ONO layer of a floating gate transistor with a first layer of silicon dioxide formed on the floating gate and a layer of silicon nitride formed on the first silicon dioxide layer, comprising:

forming a second silicon dioxide layer by thermally depositing an oxide layer on the silicon nitride layer; and

annealing the ONO layer.

2. The method of Claim 1, wherein the annealing is performed in a batch furnace at temperature range of 800 to 1150 deg Celsius for 300 seconds to 1800 seconds.

3. The method of Claim 2, wherein the annealing is performed in the batch furnace with a gas mixture of 5% to 100% of NO, with argon as a carrier gas.

4. The method of Claim 2, wherein the annealing is performed in the batch furnace with the gas mixture of 5% to 100% of NO with nitrogen as a carrier gas.

5. The method of Claim 2, wherein the annealing of is performed in the batch furnace with the gas mixture of 5% to 100% of NO with oxygen as a carrier gas.

6. The method of Claim 2, wherein the annealing is performed in the batch furnace with the gas mixture of 5% to 100% of NO with argon, nitrogen and oxygen as carrier gases.

7. The method of Claim 2, wherein the annealing is performed in the batch furnace with the gax mixture of 5% to 100% of N_2O with nitrogen as a carrier gas.

8. The method of Claim 2, wherein the annealing is performed in the batch furnace with the gas mixture of 5% to 100% of N_2O with oxygen as a carrier gas.

9. The method of Claim 2, wherein the annealing of the ONO layer is performed in the batch furnace with the gas mixture of 5% to 100% of N_2O with argon as a carrier gas.

10. The method of Claim 2, wherein the annealing of the ONO layer is performed in the batch furnace with the gas mixture of 5% to 100% of N_2O with argon, nitrogen and oxygen as a carrier gas.

11. The method of Claim 1,wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool at a temperature range of 700 to 1100 deg Celsius for one second to 120 seconds.

12. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of NO, with argon as a carrier gas.

13. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of NO, with nitrogen as a carrier gas.

14. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of NO, with oxygen as a carrier gas.

15. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of NO, with carrier gases argon, nitrogen and oxygen.

16. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of N_2O, with nitrogen as a carrier gas.

17. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of N_2O, with oxygen as a carrier gas.

18. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of N_2O, with argon as a carrier gas.

19. The method of Claim 11, wherein the annealing is performed in a single wafer Rapid Thermal Annealing tool with a gas mixture of 1% to 100% of N_2O, with carrier gases argon, nitrogen and oxygen.

20. The method of Claim 1, wherein the second silicon dioxide layer is formed by rapid thermal chemical vapor deposition (RTCVD) process.

21. The method of Claim 20, wherein said RTCVD process occurs in a single wafer tool.

22. The method of Claim 1, wherein the second silicon dioxide layer is formed by low pressure chemical vapor deposition (LPCVD) process.

23. The method of Claim 22, wherein said LPCVD process occurs in a batch furnace.

24. The method of Claim 1, wherein the floating gate transistor is in a flash memory device.

25. The method of Claim 24, wherein the flash memory device is an EEPROM device.